Semicon Japan 2005

Characterization and Production Testing at 3.2-5.0 Gb/s for PCI Express™ II and FB DIMM

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Wavecrest Corporation

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Purposes

- Review high-speed I/O basic test methods
- Review PCIe II and FB DIMM test requirements
- Illustrate test methods meeting the requirements
- Illustrate test methods and apparatus covering both design verification and production
- Illustrate case study examples for actual devices to prove the methods

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Outline

I. High-speed I/O test review
- Link architecture evolution
- jitter, noise, and signaling
- BER and interoperability

II. PCIe II and FB DIMM test requirements
- Link architecture overview
  - Jitter, noise, and BER (JNB) transfer functions
  - JNB and signaling tests (Tx, Rx, and Ref clock)

III. Test methods meeting requirements
- Transmitter
- Receiver
- PLL
- Ref clock

IV. Applications and case studies
- Compliance test
- Test from design verification to production

V. Summary and conclusion

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I: High Speed I/O Test Review

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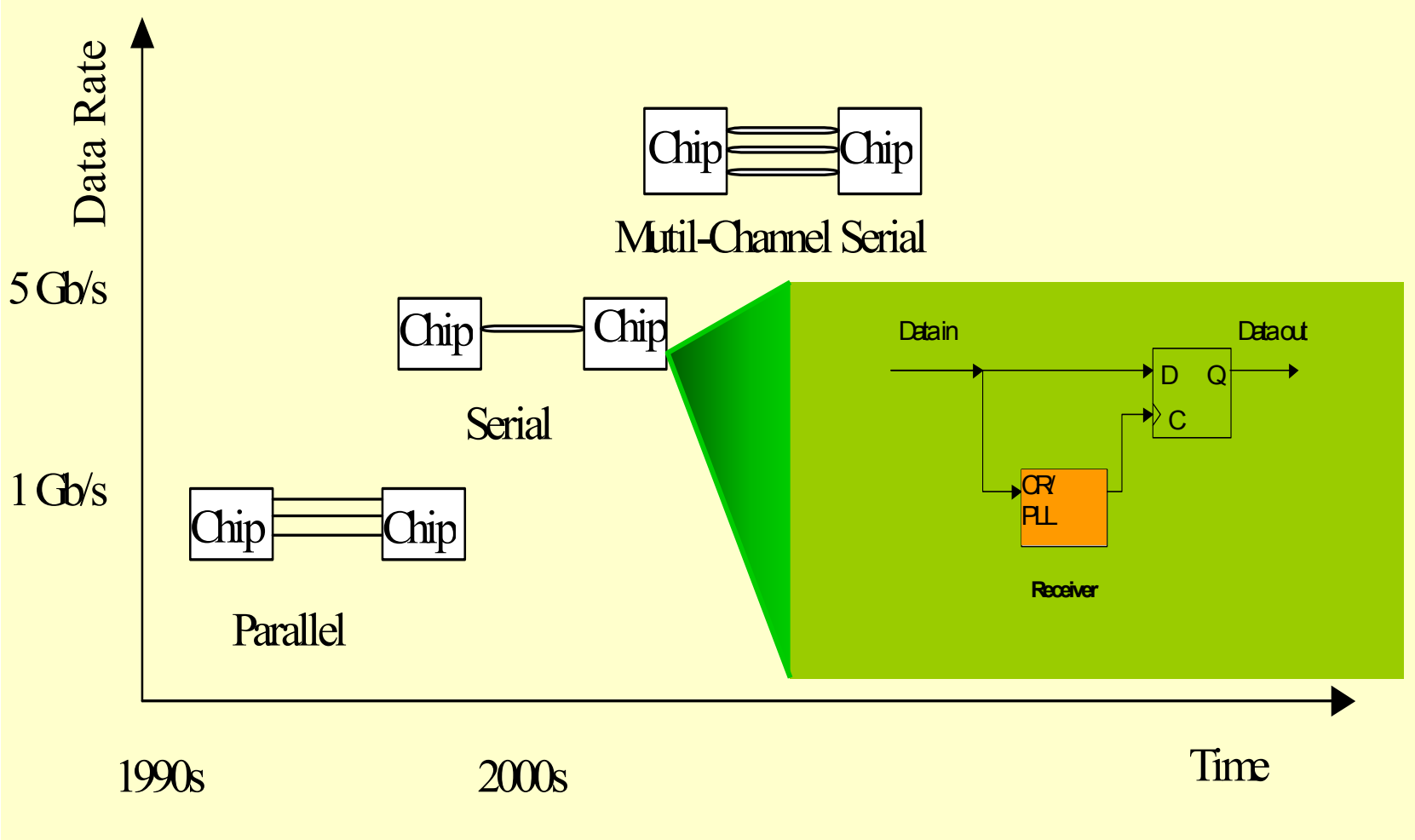
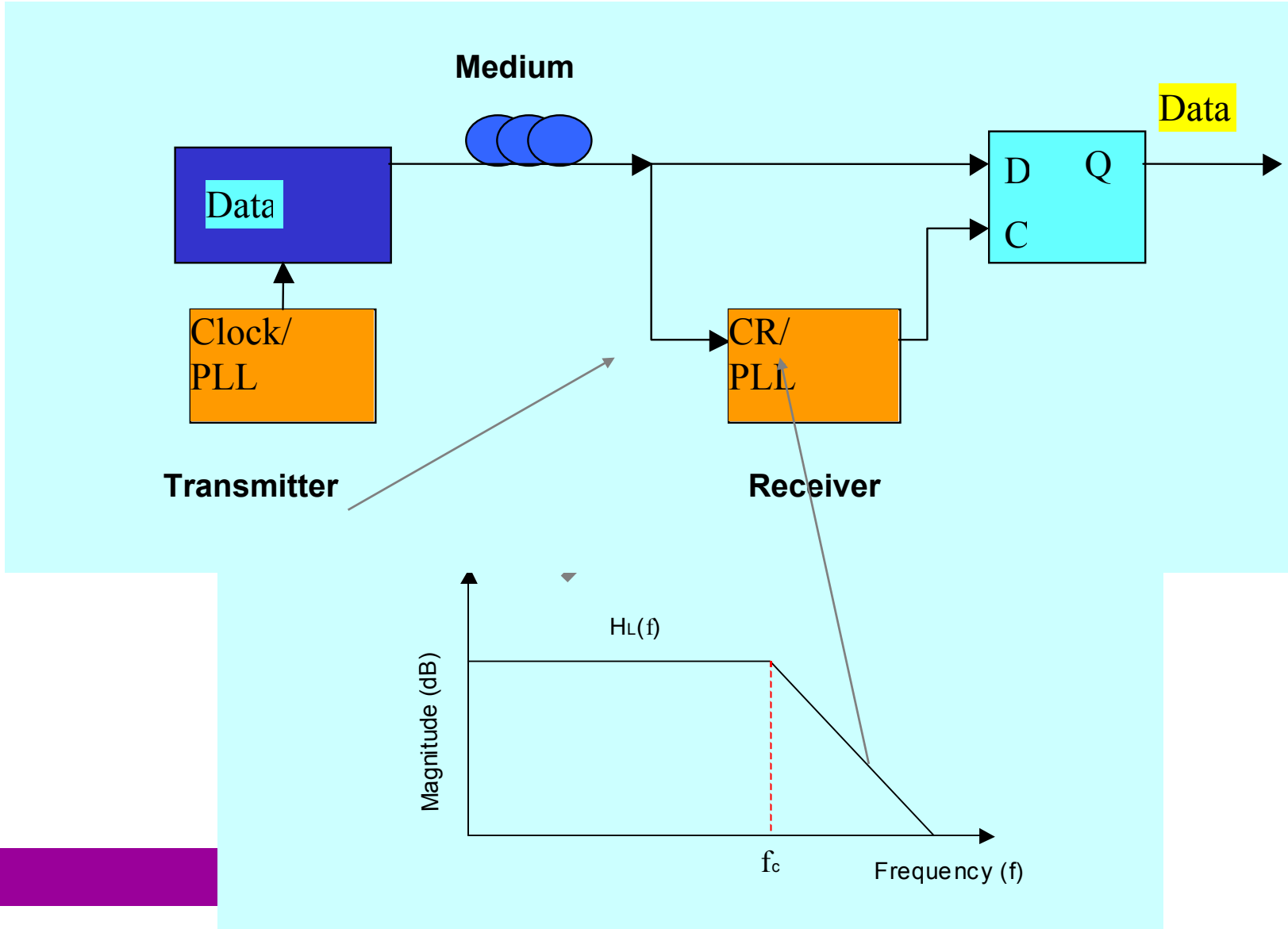
Short-Haul (~ m) Link Technology Trend

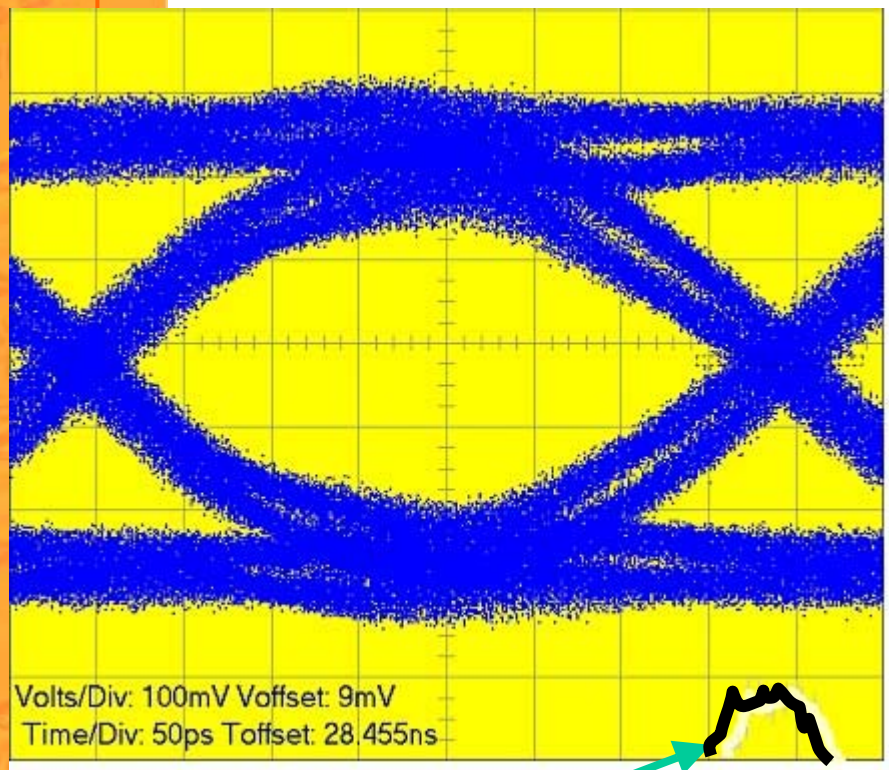


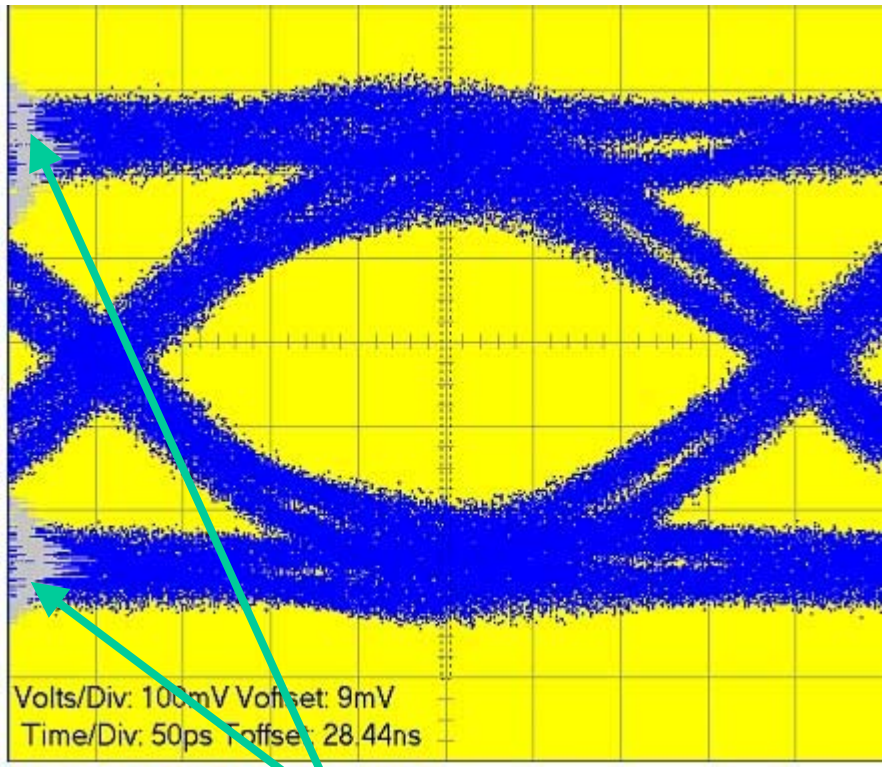
A Serial Data Communication System



Timing Jitter, Amplitude Noise, and BER (JNB)

- Timing jitter and amplitude noise can both cause bit errors to occur
- Bit Error Rate (BER) needs to be 10^{-12} or smaller
- Interoperability is merited by jitter, noise, and BER





Timing jitter pdf

Amplitude noise pdf

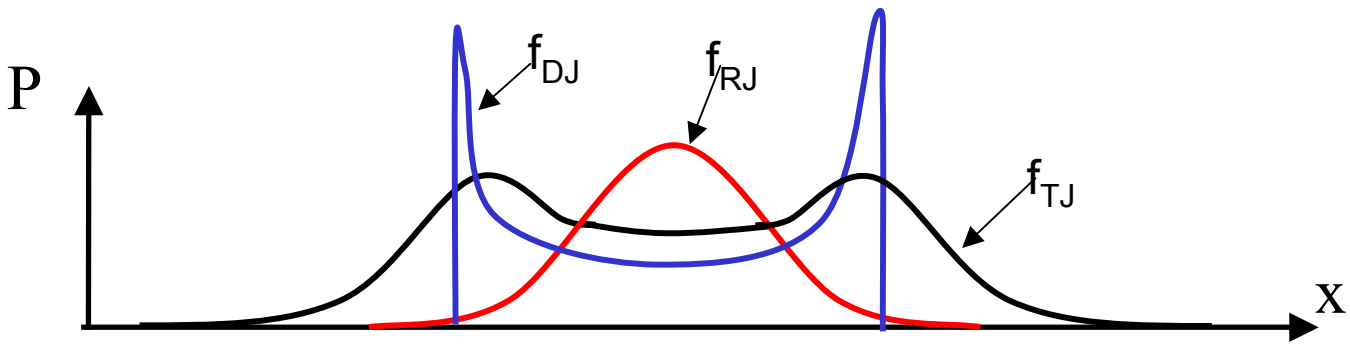
Law for PDFs: Convolution

- Convolution is defined by the following equation:

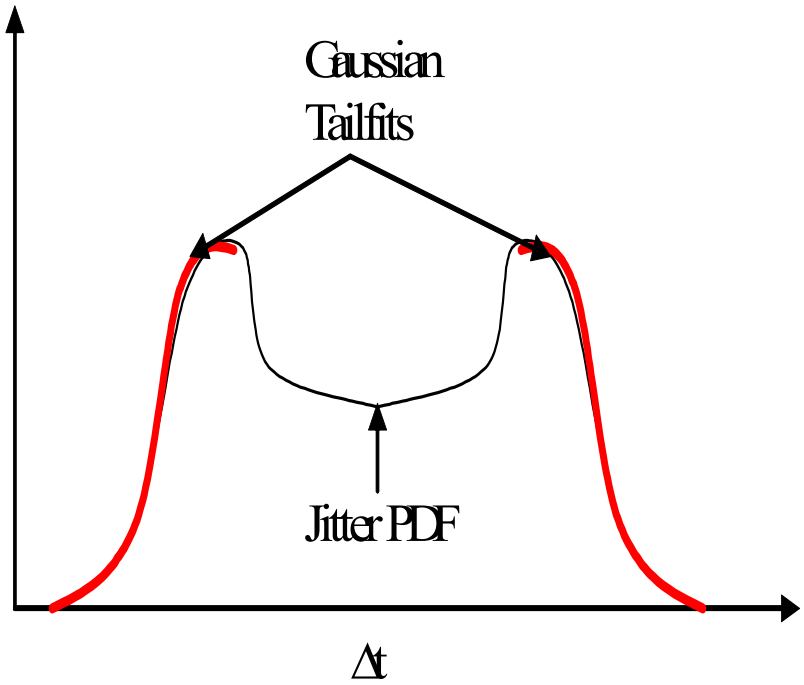
$$f(x) * g(x) = \int_{-\infty}^{+\infty} f(u)\, g(x-u)\, du$$

- The Total Jitter PDF is equal to the convolution of RJ PDF with the DJ PDF. This is shown in this equation:

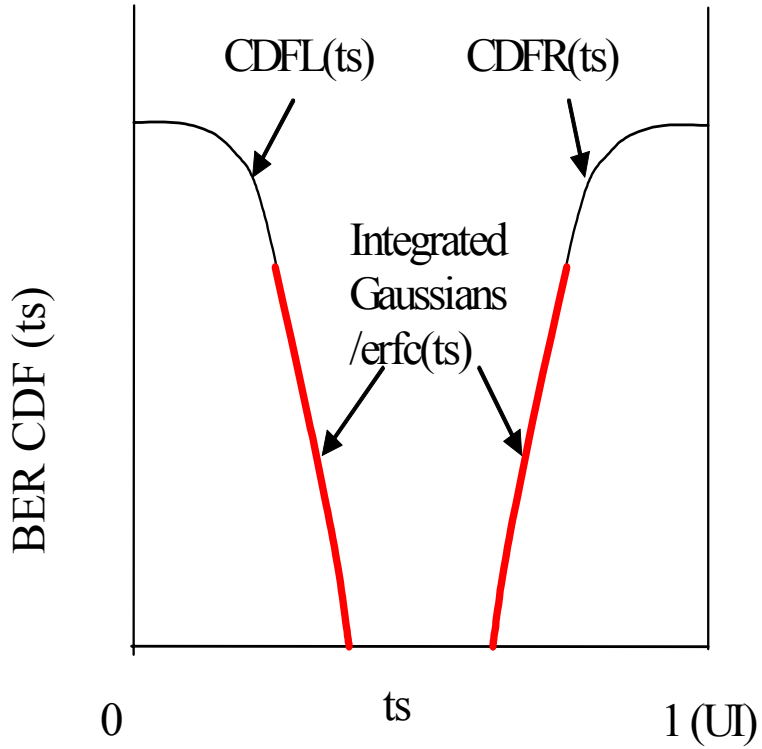
$$f_{TJ}(x) = f_{RJ}(x) * f_{DJ}(x) = \int_{-\infty}^{\infty} f_{RJ}(u) \cdot f_{DJ}(x-u)\, du$$



Jitter Separation (I): PDF or BER CDF Domain with TailFit

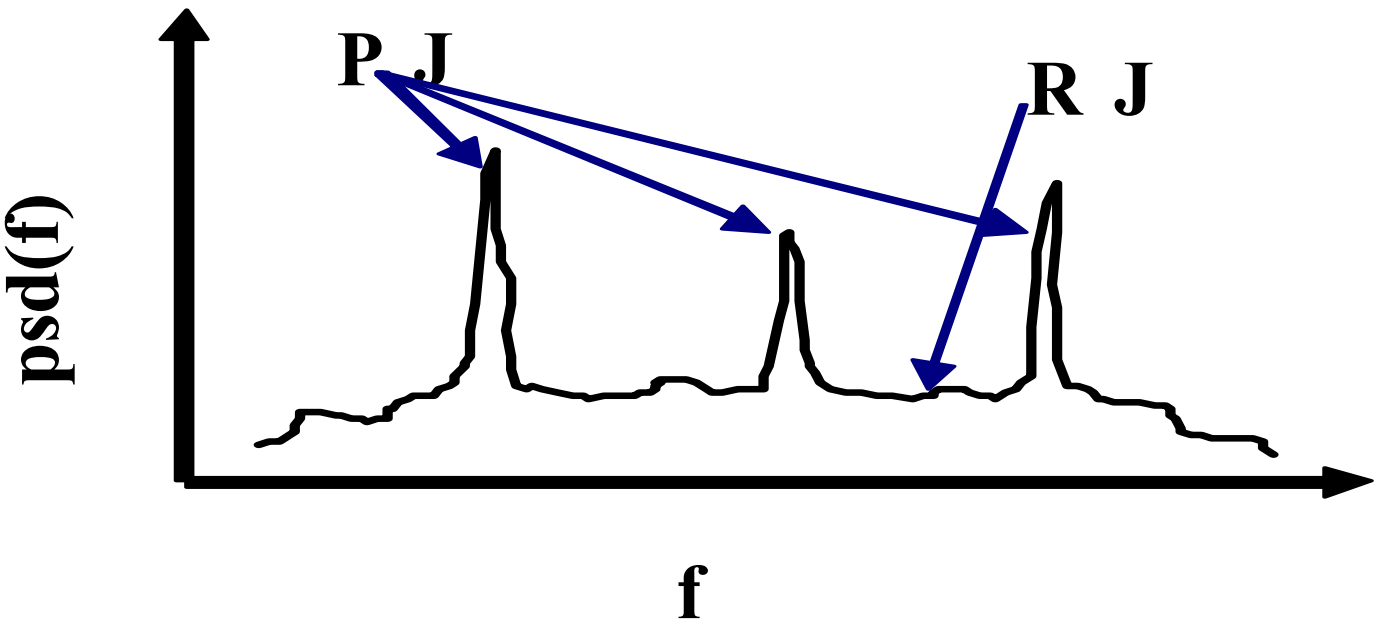


(a)



(b)

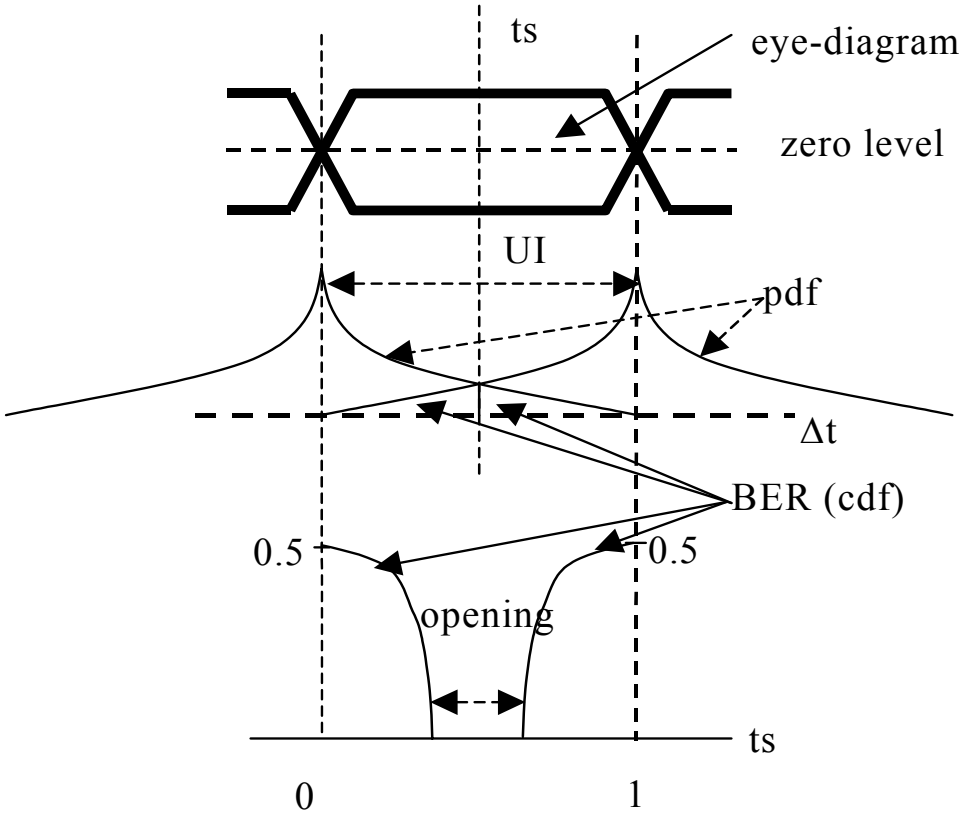
Jitter Separation (II): Time or Frequency Domain with Autocorrelation or PSD



- RJ PSD
- PJ PSD
- DDJ (DJ without PJ and BUJ) PSD

Jitter PDF, BER CDF, and Eye-Diagram

- Relationship of Eye Diagram, TJ PDF and BER CDF



$$BER(t_s) = \frac{1}{2}[\int_{t_s}^{\infty} f_{TOT}(t)dt + \int_{-\infty}^{t_s} f_{TOT}(t - UI)dt]$$

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II: PCIe II and FB DIMM Test Requirements

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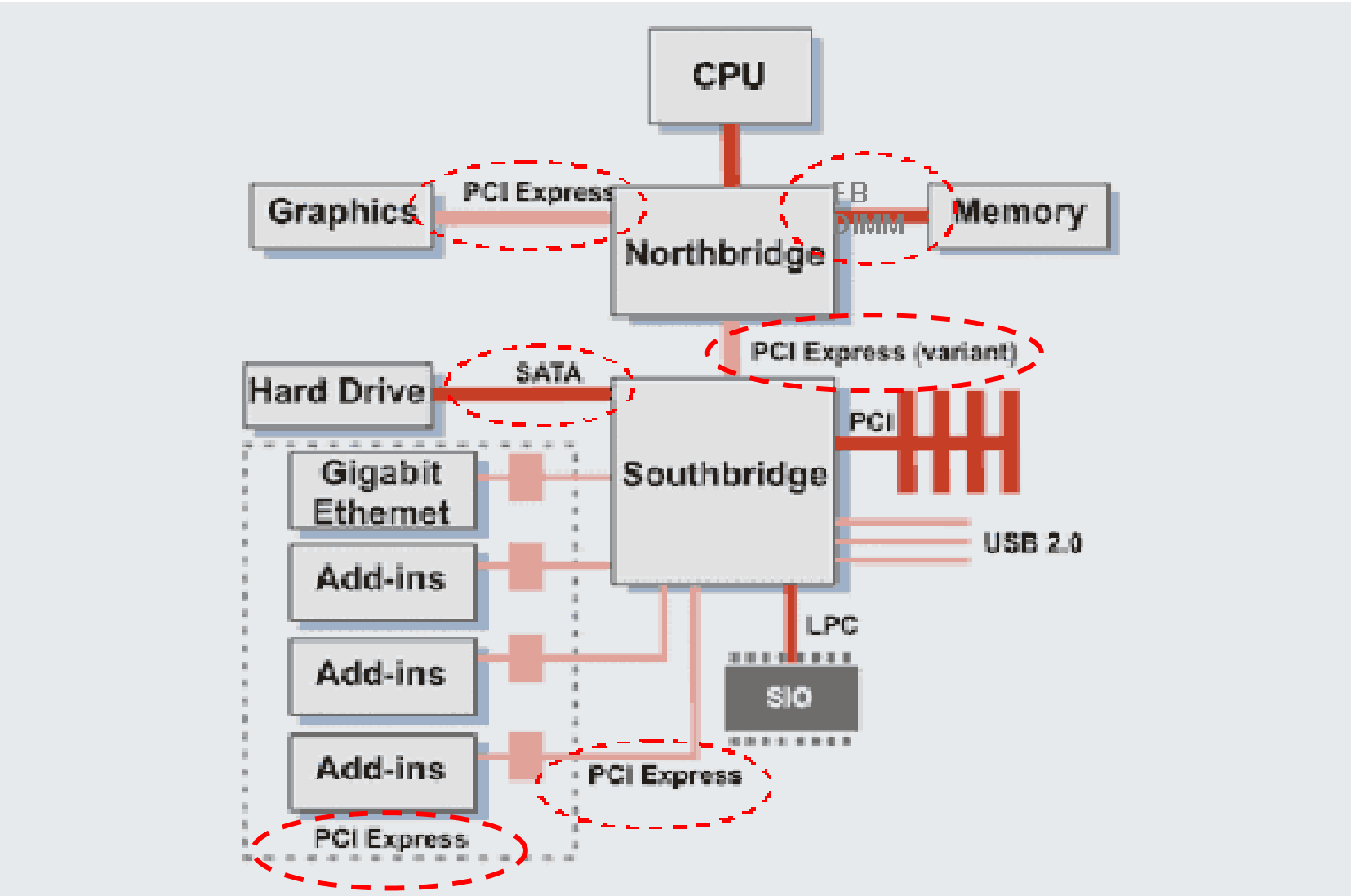
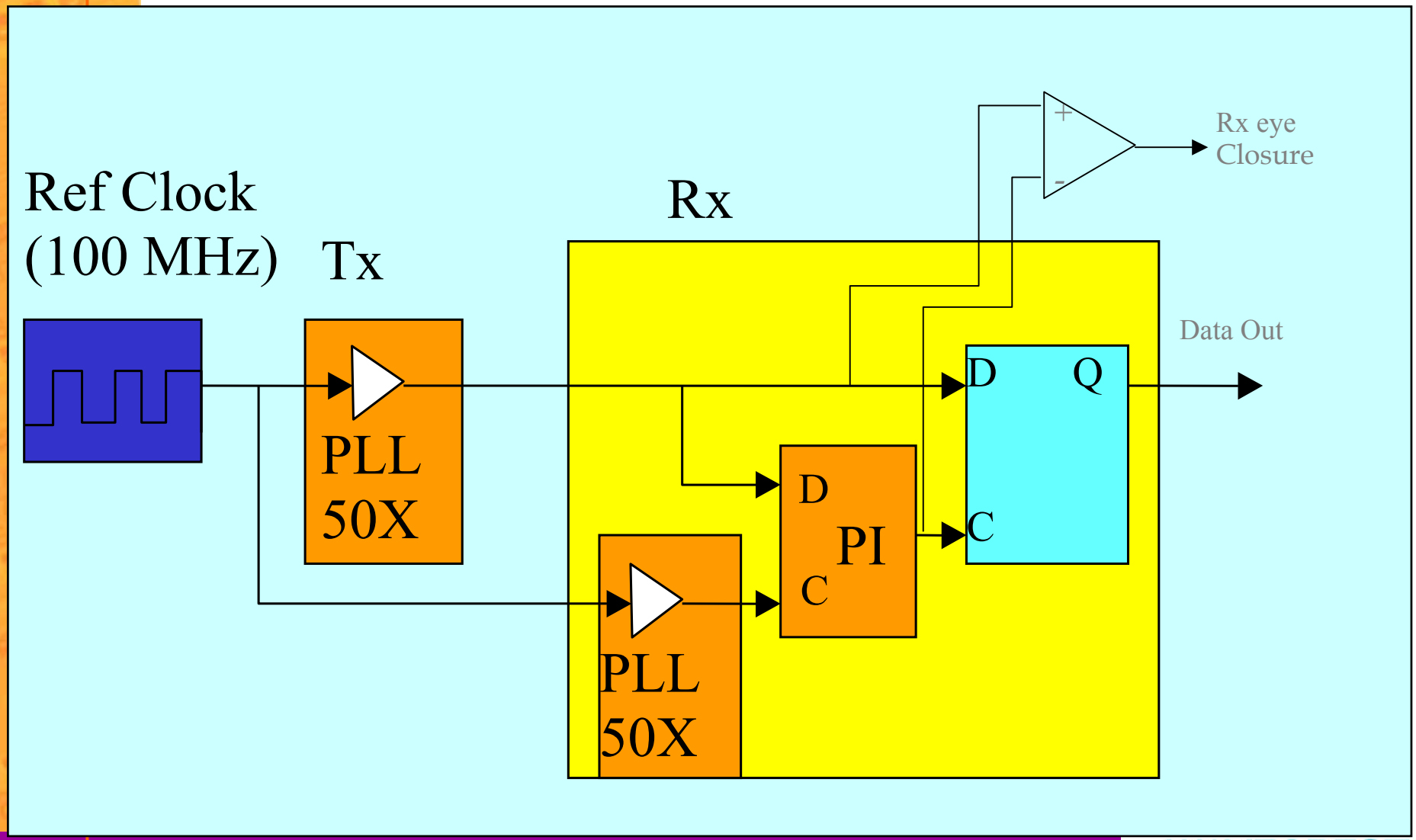
PCI Express Applications



PCIe II Link Architecture (PI or OS Based)



PCIe II Basic Data Sheet

- Data Rate: 5.0 Gb/s
- UI: 200 ps $\pm$ 300 ppm
- Reference clock: 100 MHz
- PLL multiplication: 50X

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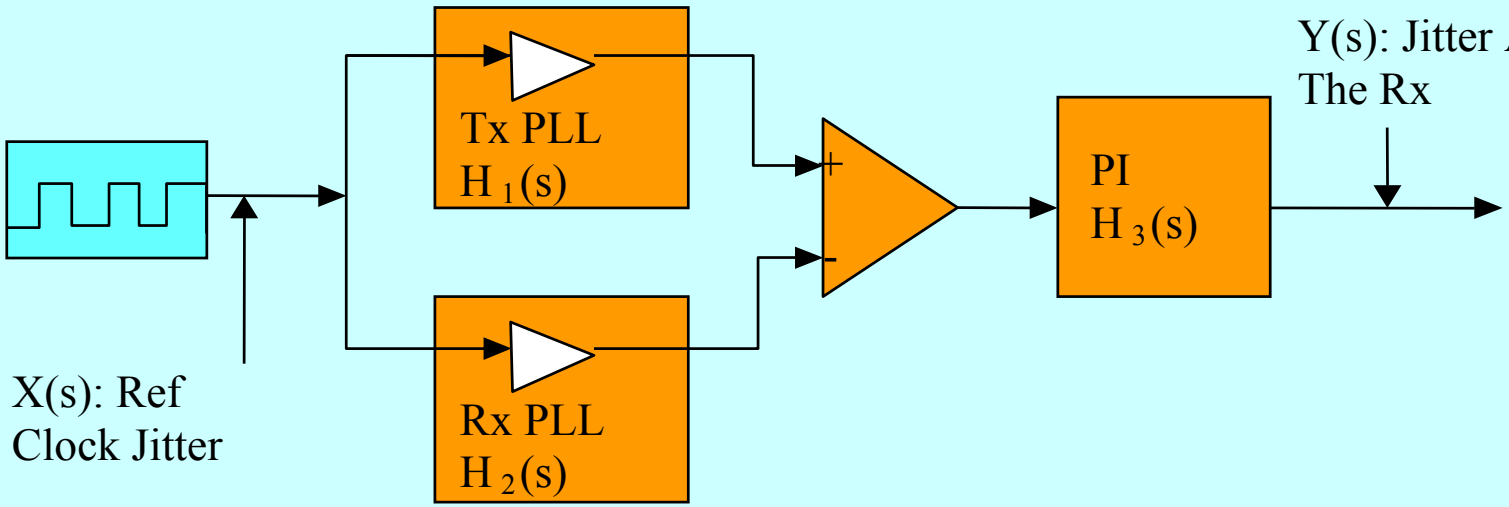
System Transfer Functions



$$Y(s) = H_t(s)X(s) = \{[H_1(s)e^{-sT_d} - H_2(s)]H_3(s)\}X(s)$$

Tx Amplitude Voltage Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
VTX-DIFF-PP	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	**0.8 (min)** **1.2 (max)**	V
VTX-DE-RATIO -	Tx de-emphasis level	3.0 (min) -4.0 (max)	**-5.5 (min)** **-6.5 (max)**	dB

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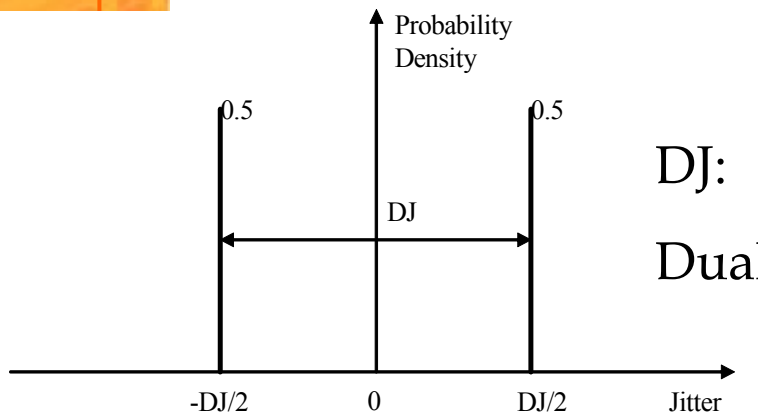
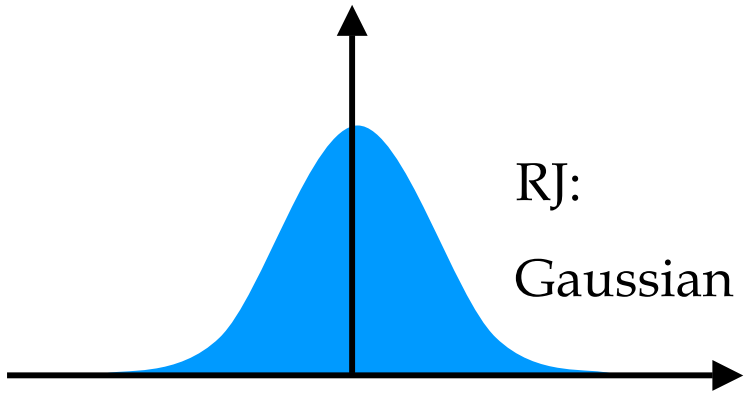
Tx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
TMIN-PULSE	Instantaneous pulse width	Not spec'ed	**0.9 (min)**	UI
TTX-EYE	Transmitter Eye opening (@10^{-12} BER) including all jitter sources	0.75 (min)	**0.75 (min)**	UI
TTX-DJ-DD (max)	Tx deterministic jitter (DJ)	Not spec'ed	**0.15 (max)**	UI



DJ:

Dual-Dirac



RJ:

Gaussian

Tx PLL Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
BWTX-PLL	Maximum Tx PLL Bandwidth (BW)	22 (max)	**16 (max)**	MHz
BWTX-PLL-LO-3DB	Minimum Tx PLL BW for 3 dB peaking	3 (min)	**8 (min) MHz**	MHz
BWTX-PLL-LO-1DB	Minimum Tx PLL BW for 1 dB peaking	Not spec'ed	**5 (min)**	MHz
PKGTX-PLL1	Tx PLL peaking with 8 MHz min BW	Not spec'ed	**3.0 (max)**	dB
PKGTX-PLL2	Tx PLL peaking with 5 MHz min BW	Not spec'ed	**1.0 (max)**	dB

Tx Test Jitter Transfer Function

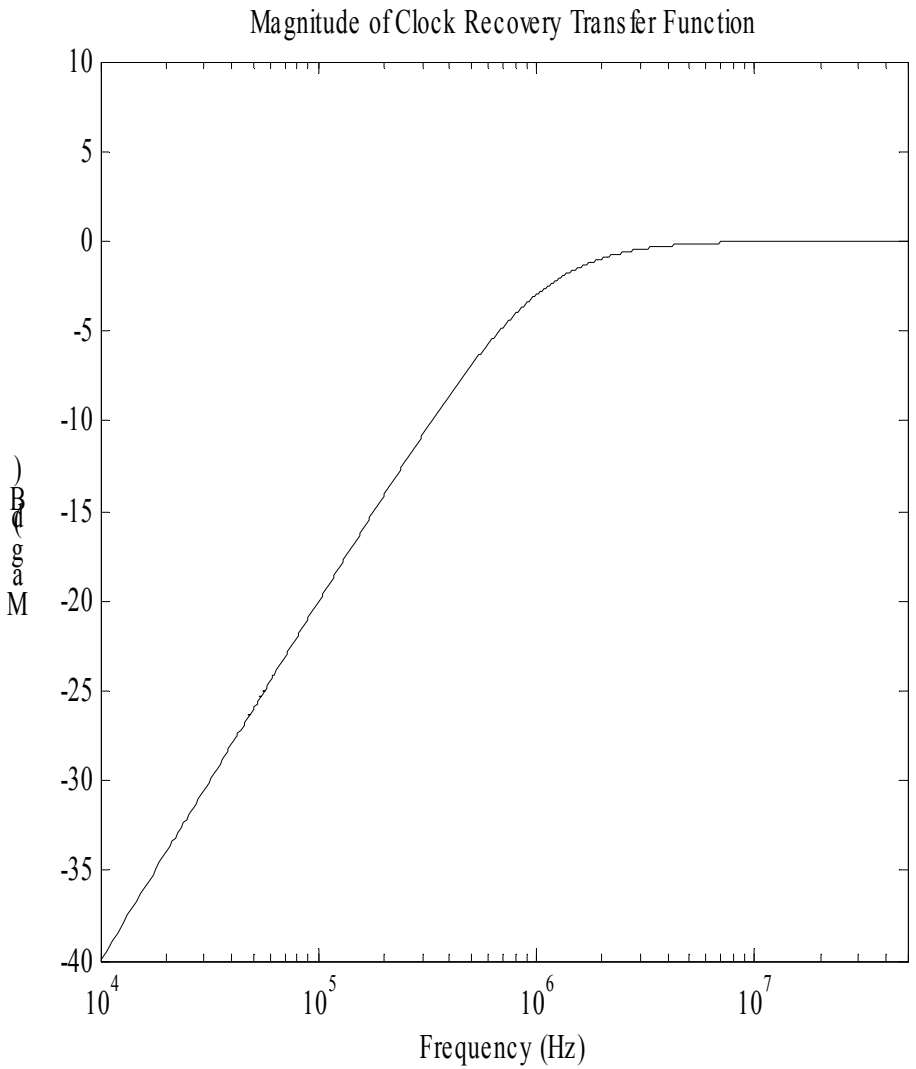
1st -order HPF of

$$H_3(s) = \frac{s}{s + \omega_3}$$

$$\omega_3 = 2\pi f_3$$

where

$$f_3 = 1.0\,MHz$$



Reference Clock Test Requirements

Symbol	Parameter and Definition	Min	Max	Unit
TPERIOD-ABS	Averaged instantaneous period (including SSC)	9.997	10.053	ns
VIH VIL	Differential Input High Voltage Differential Input Low Voltage	+150	-150	mV
VRB	Ring-back Voltage Margin	-100	+100	mV
$(dV/dt)_R$	Rising Edge Rate	0.6	4.0	V/ns
$(dV/dt)_F$	Falling Edge Rate	0.6	4.0	V/ns
η_{DC}	Duty Cycle	40	60	%
TCLK_RJ	**Ref clk RMS jitter**		**3.1**	**ps**
TSSC-JITTER-CC	SSC induced jitter that a receiver must track. Relevant only for common clock architecture		65 ps PP at 33 KHz	ps
TSSC-JITTER-DDC	SSC induced jitter that a receiver must track. Relevant only for data driving PLL architecture		20 ns PP at 33 KHz	ns

Reference Clock Jitter Transfer Function

$$H(s) = \left[H_1(s) * e^{-s * t\_delay} - H_2(s) \right]$$

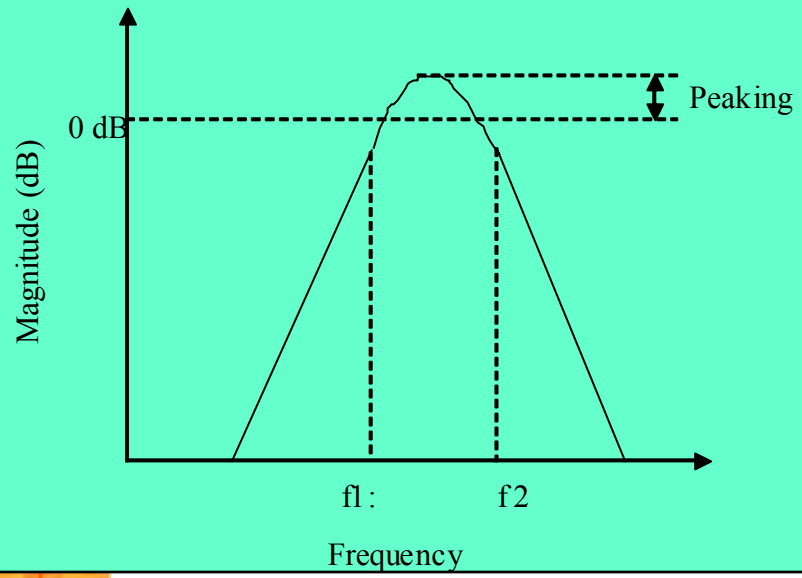
$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2}$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2}$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2*\pi*8.61*10^6}{\sqrt{1+2\zeta^2+\sqrt{\left(1+2\zeta^2\right)^2+1}}} Rad/s$$

$$\omega_2 = \frac{2*\pi*4.31*10^6}{\sqrt{1+2\zeta^2+\sqrt{\left(1+2\zeta^2\right)^2+1}}} Rad/s$$



$$t\_delay = 12 \cdot 10^{-9}\, s$$

Rx Amplitude Voltage Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
VRX-DIFF-PP	Differential p-p Rx voltage swing	0.175 (min) 1.2 (max	**0.120 (min)** **1.2 (max)**	V
VRX-MAX-MIN-RATIO	Max to Min pulse voltage on consecutive UI	Not spec'ed	**5 (max)**	

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Rx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
TRX-EYE	Receiver Eye opening (@10^{-12} BER)	0.4 (min)	**0.4 (min)**	UI
TRX-DJ-DD (max)	Rx deterministic jitter (DJ)	Not spec'ed	**0.44 (max)**	UI

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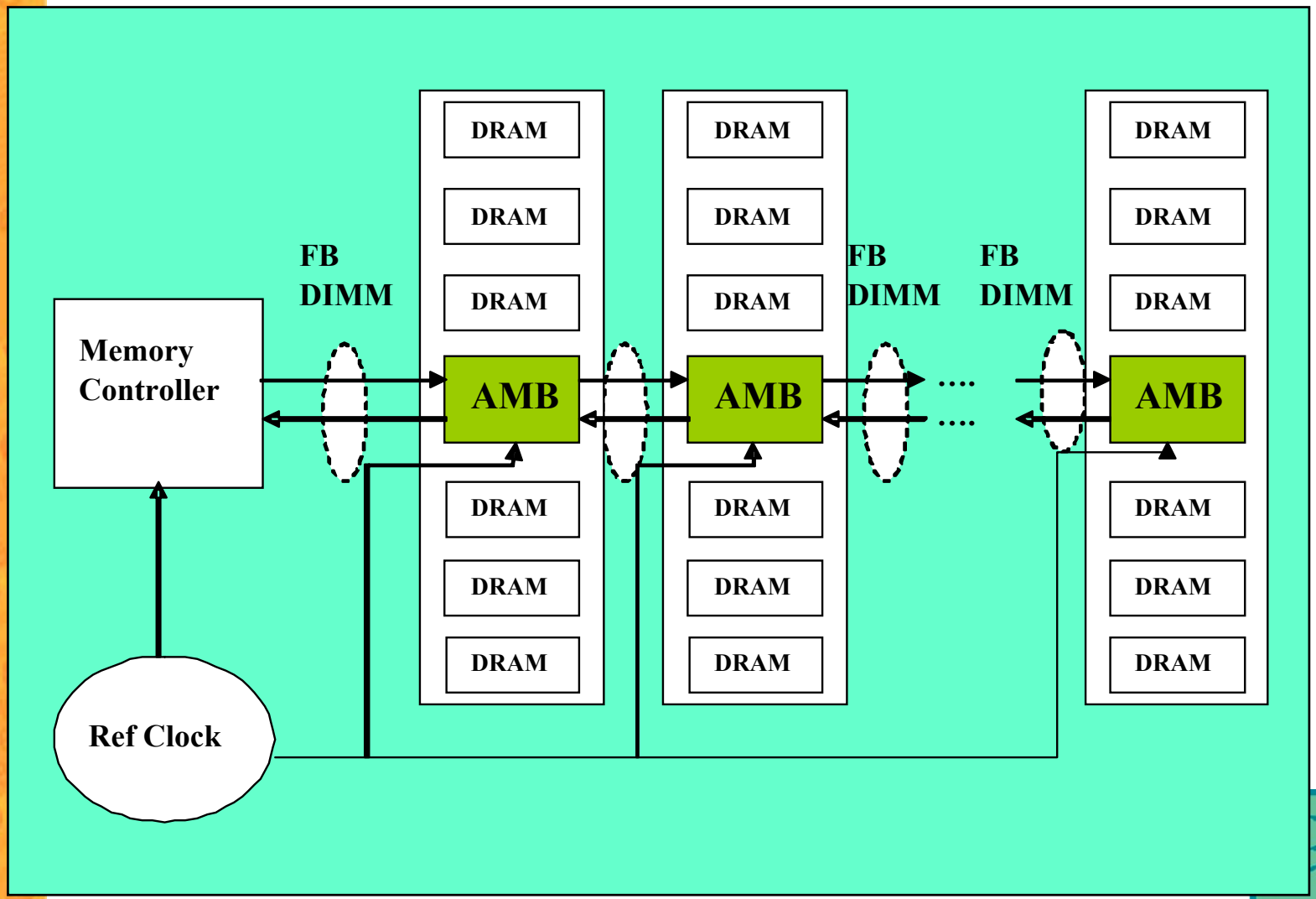
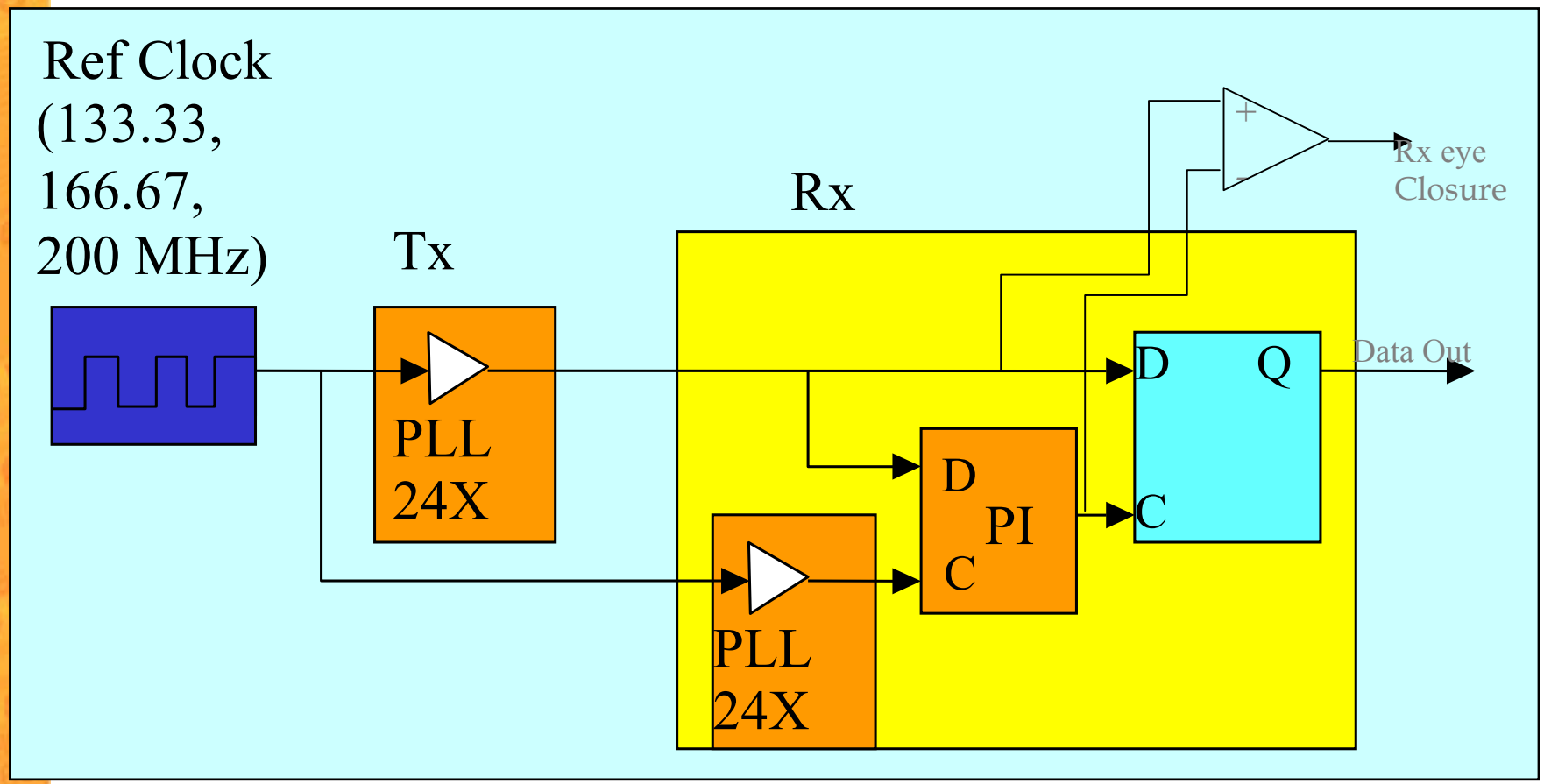
FB DIMM Applications



FB DIMM Link Architecture



- Very similar to PCIe
- Resulting in similar test requirements

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FM DIMM I Basic Data Sheet

- Data Rate: 3.2, 4.0, 4.8 Gb/s
- UI: 312.5, 250, 208.33 ps
- Reference clock: 133.33, 166.67, 200 MHz
- PLL multiplication: 24X

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III: Test Methods Meeting Requirements

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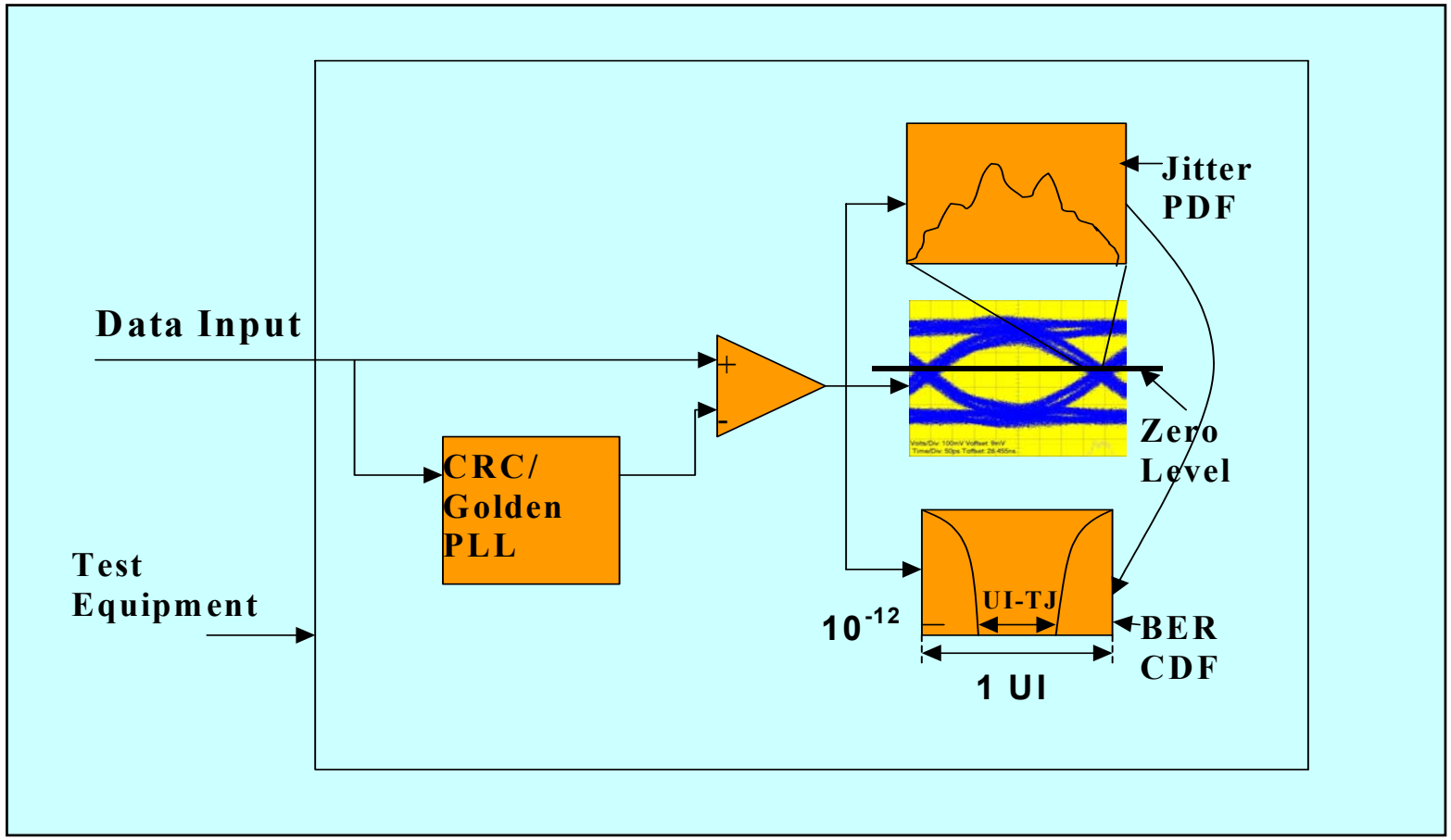
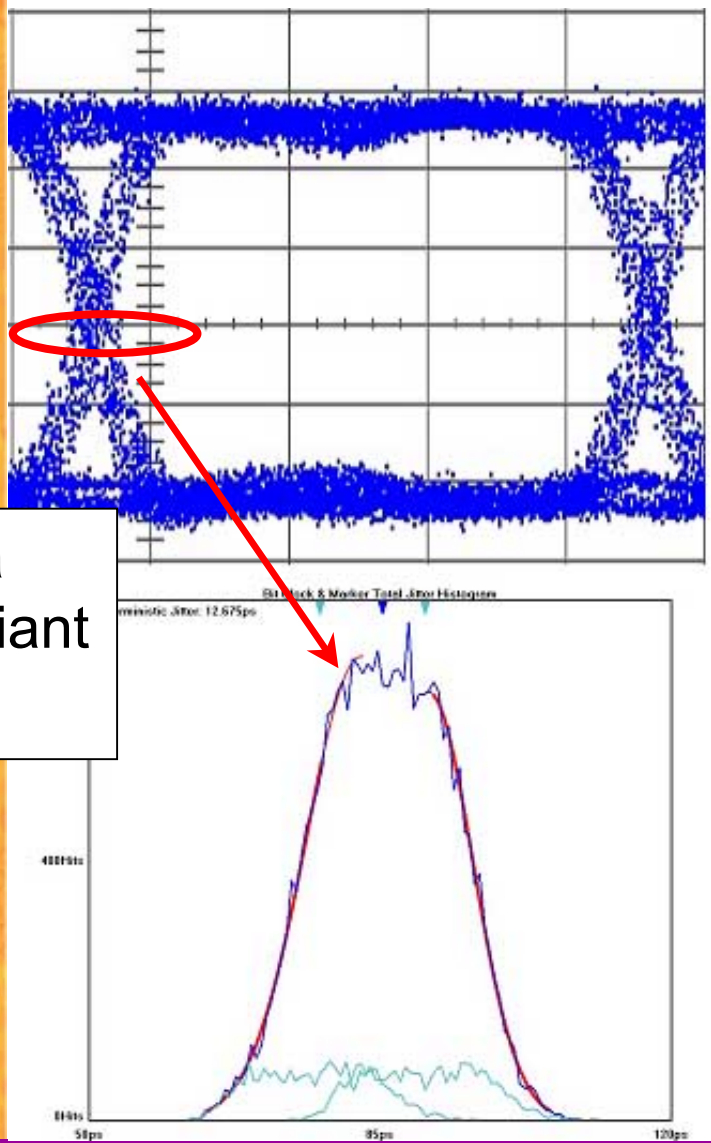
Tx Jitter/Signaling Test Methods

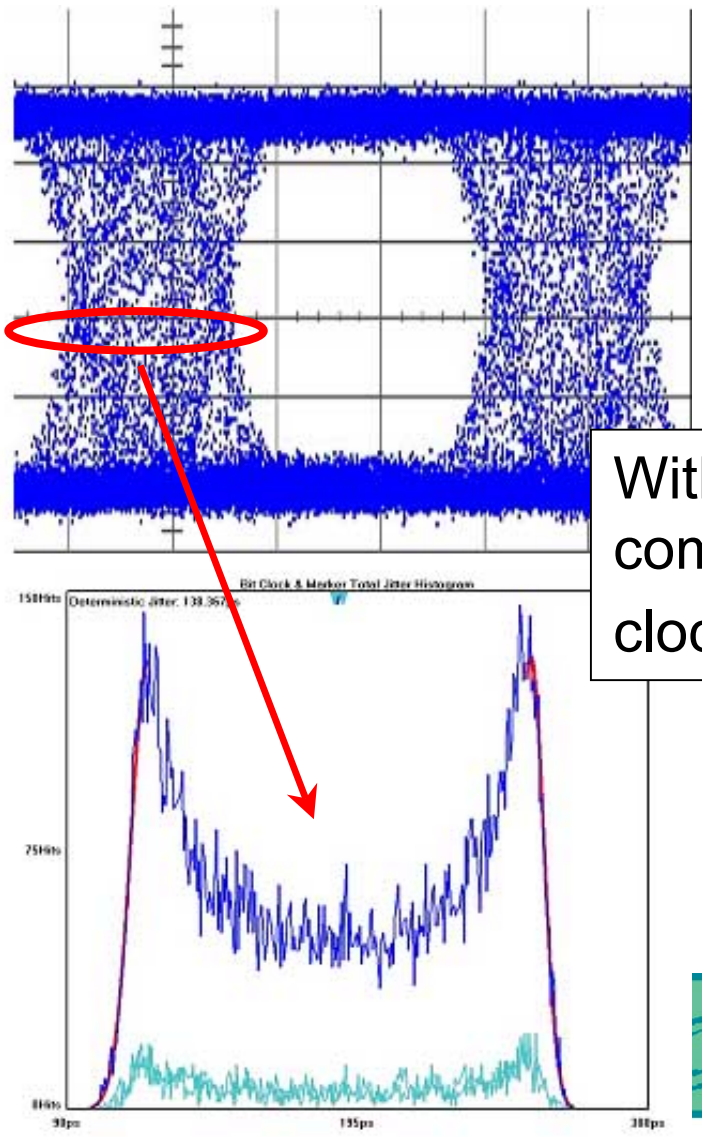
- Measure clock-to-data jitter
- TJ is measured at BER = 10^{-12}



Tx Test: Effect of Clock Recovery



With a compliant clock



Without a compliant clock

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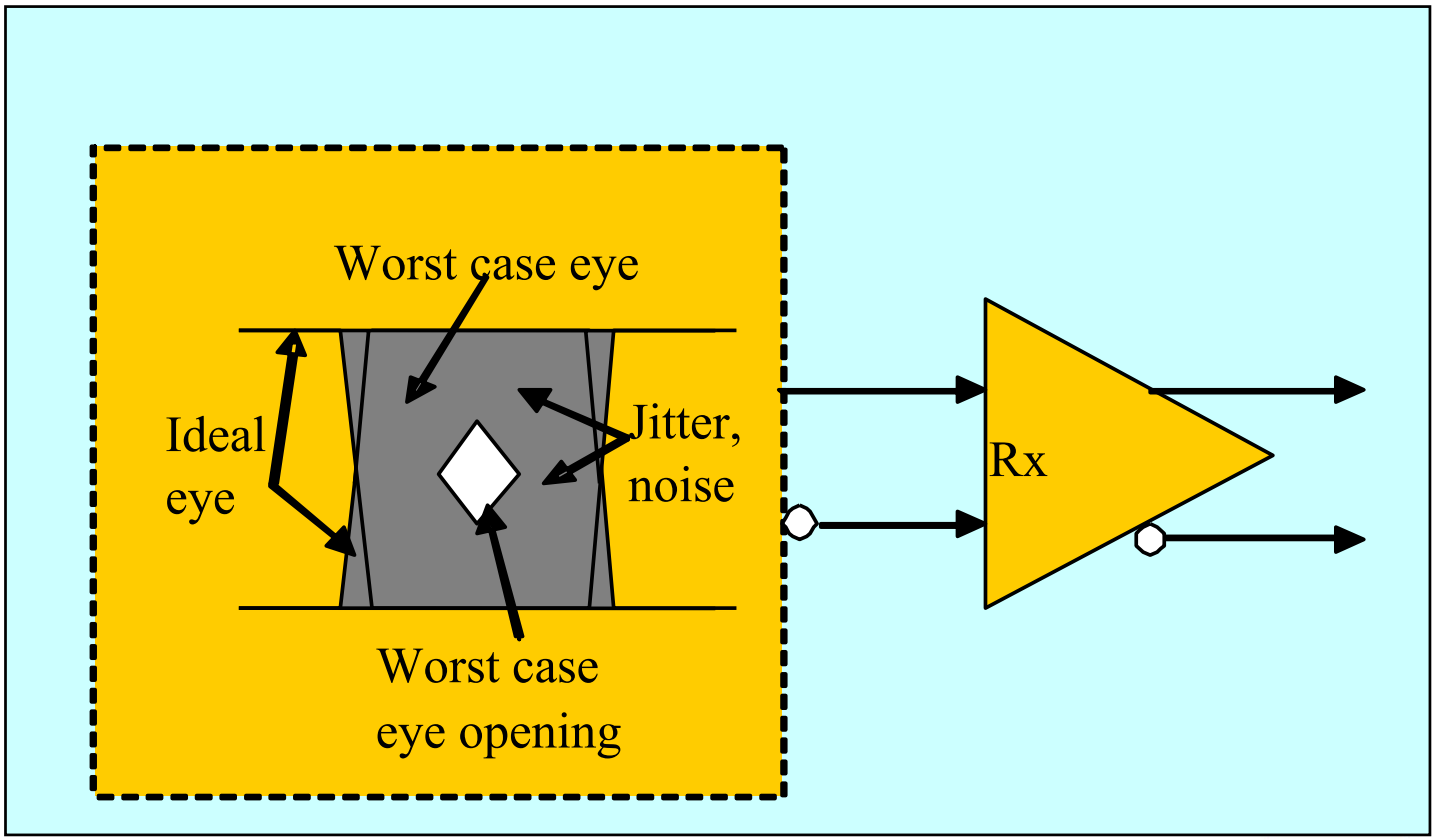
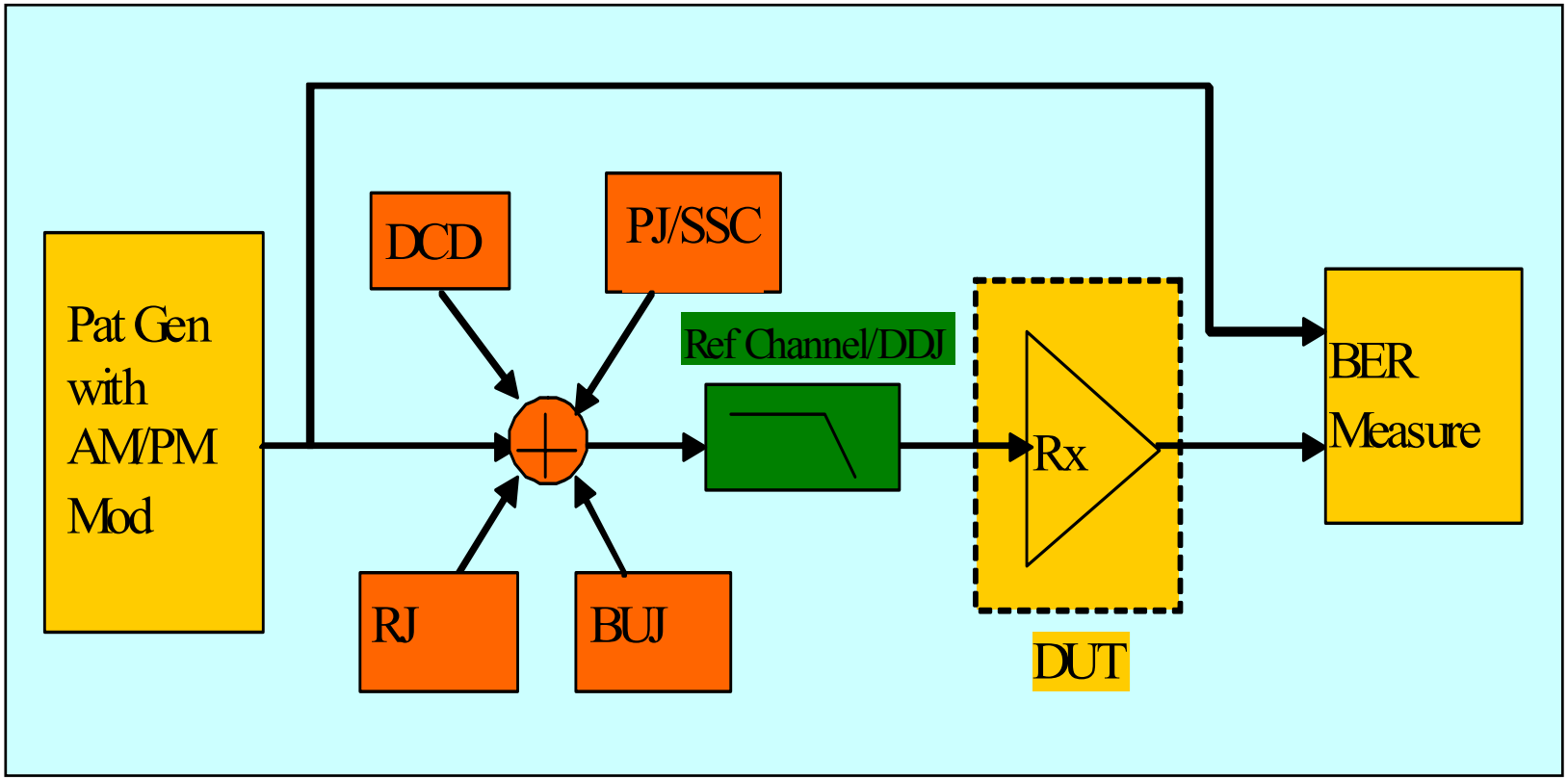
Rx Jitter/Signaling Test Methods

- Create the worst jitter/signaling conditions to stress the Rx and insure that it still meets the 10^{-12} BER requirement



Rx Jitter/Signaling Test Method Cont...



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PLL Test Methods

- Measure the PLL jitter variance function to derive the PLL transfer function (No need for a stimulus, in-situ measurement, Wavecrest patented technology)
- Measure the step response of the PLL (Needs a stimulus)
- Frequency sweeping (Needs a stimulus, magnitude only and slow)

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Reference Clock Jitter Test Methods

- Step 1: Measure the phase jitter time record, or spectrum, or power spectrum density (PSD)
- Step 2: Apply the required filter function in either time-domain, or frequency-domain
- Step 3: Estimate the RMS value after the filter function.

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IV: Application and Case Study Examples

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Equipment Used

- New Wavecrest SIA-4000:
- Up to 10 Gb/s data rate, 15 GHz bandwidth
- DJ < 5 ps typical, RJ < 200 fs rms (band limited)
- Rise time: 20 ps
- 8 SE/DIFF built-in channels, extendable to 32, 64, 128, 256… etc. via relay matrix
- < 50-100 ms throughput per channel for most of the SERDES compliance tests

SIA-4000

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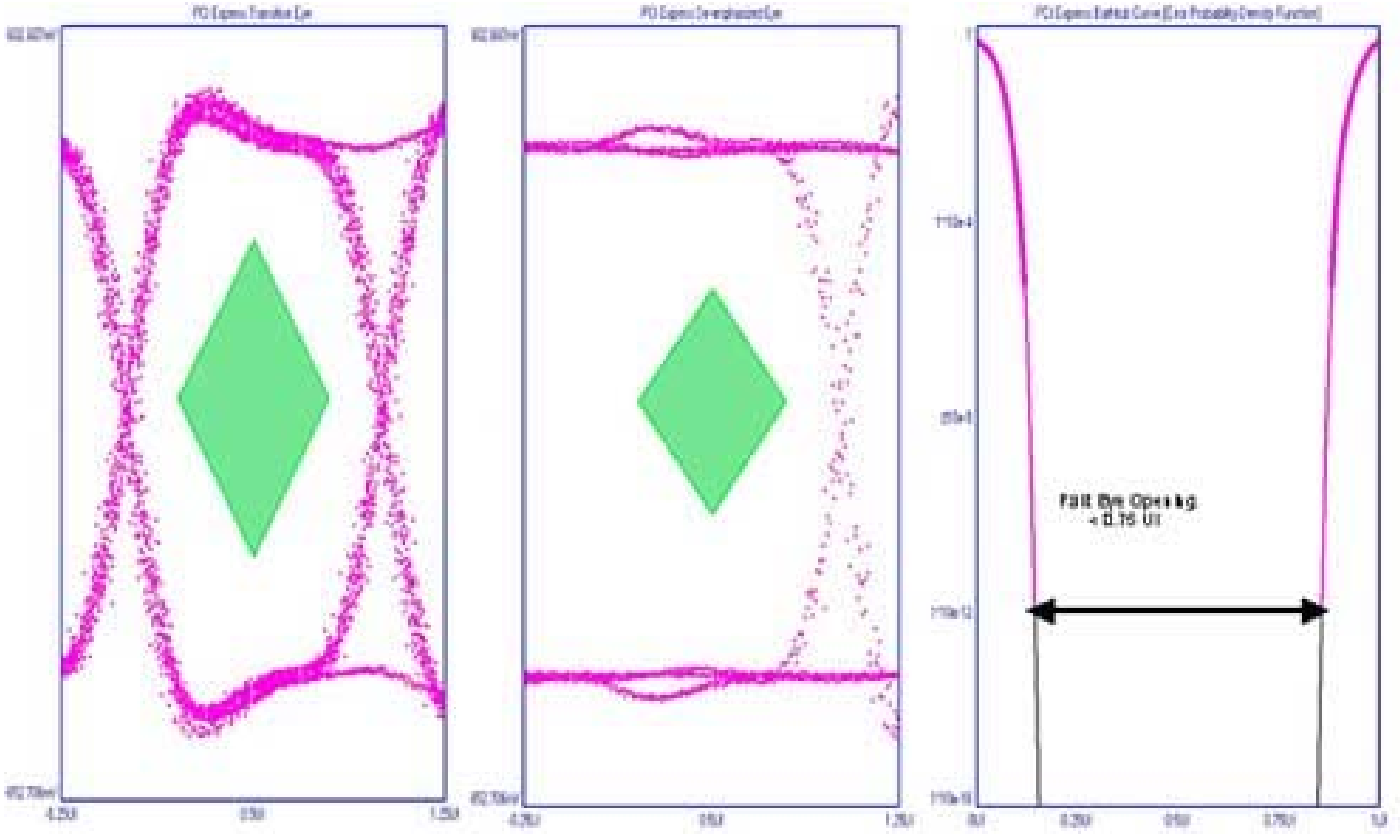
Tx JNB Compliance Test Example (PCIe II)



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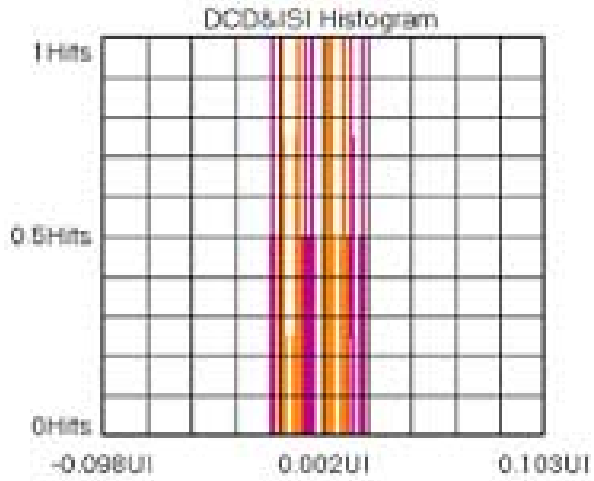
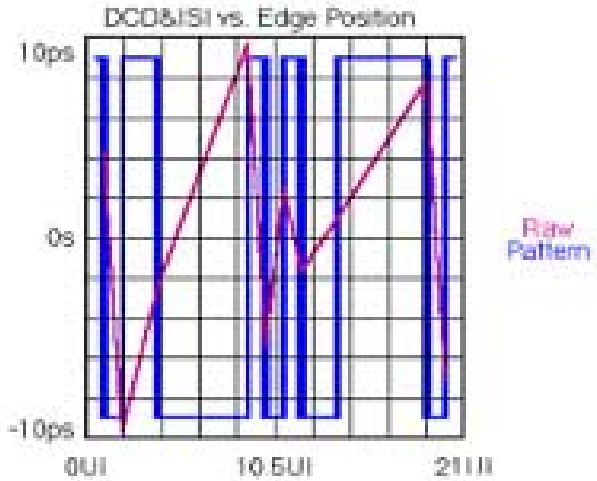
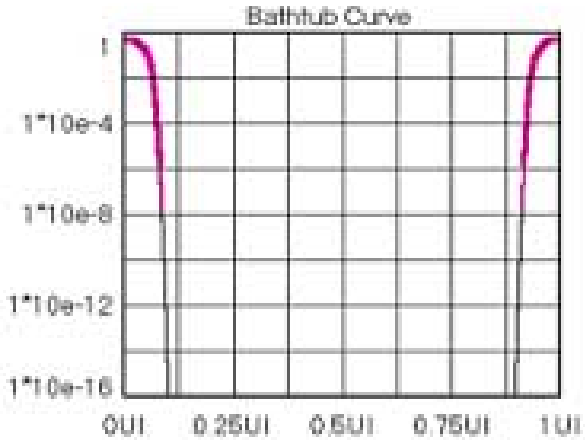
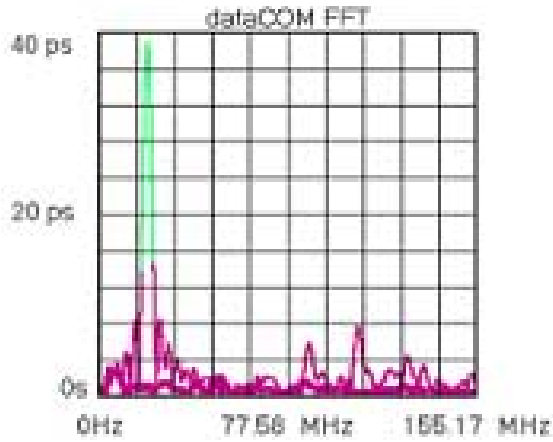
Tx JNB Diagnostic Test Example (PCIe II)









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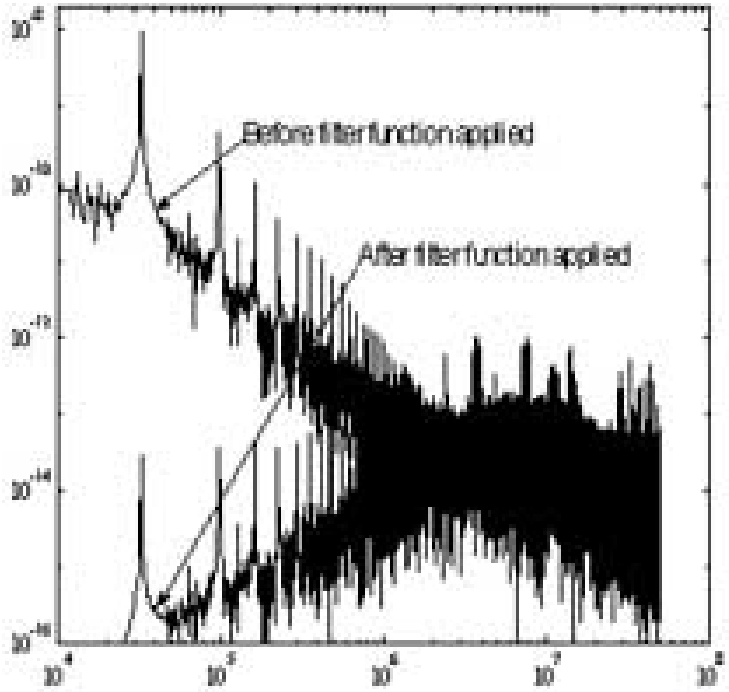
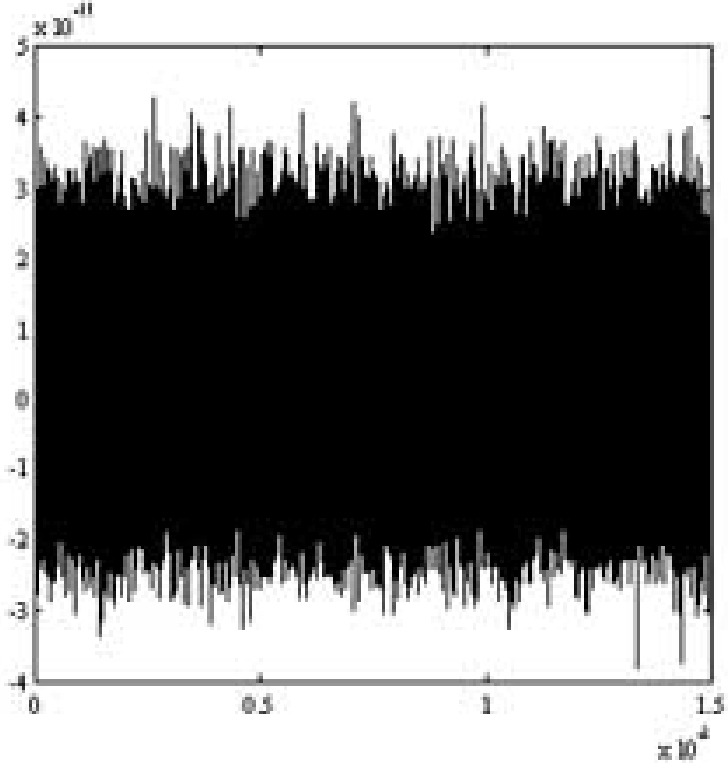
Reference Clock Test Example (PCIe II)





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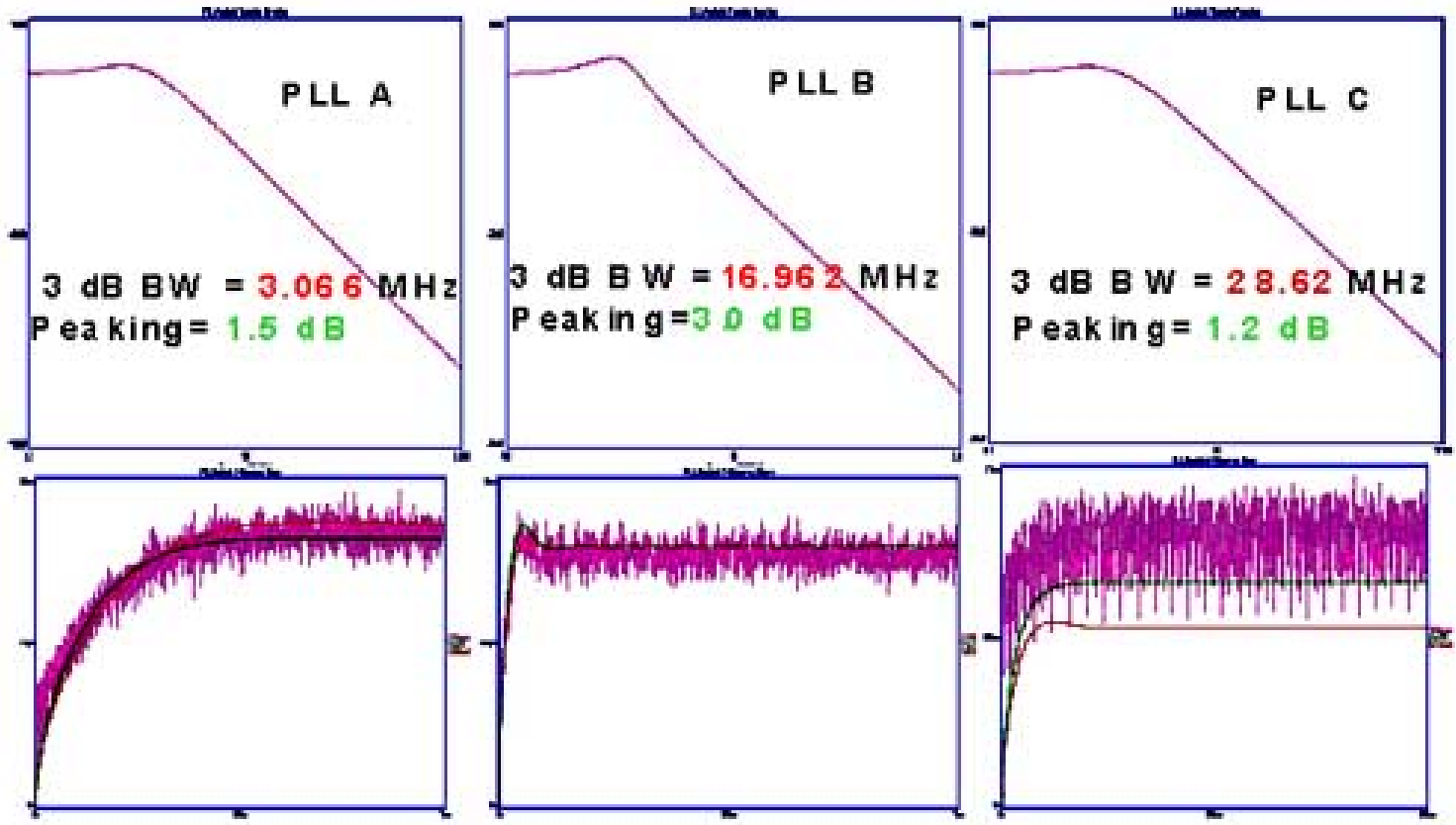
PLL Test Examples (PCIe II)



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Other High-Speed I/O Link Tests

- FB DIMM link architectures are not much different from that of PCI Express
- Test Methods illustrated can apply well for those and similar link standards

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V. Summary and Conclusion

- High-speed I/O *trend and testing* are reviewed
- PCIe II and FB DIMM test requirements are presented
- *Test methods* meeting those new requirements are illustrated
- *Case study examples* are demonstrated for tests of *compliance and diagnostic*, as well as *design verification and production*
- Test methods introduced *can also be applied* to *other I/O links* such as SATA, Fibre Channel (FC), 10 Gigabit Ethernet (GBE), etc.

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